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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,704	10/31/2003	Robert O. Conn	X-1416-3 US	1939

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,704	CONN, ROBERT O.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☐ This action is **FINAL**. b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 12-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/698704 Attorney's Docket #: X-1416-3US
Filing Date: 10/31/2003;

Applicant: Conn Examiner: Alexander Williams

Applicant's Response filed 10/10/06 to the election of Group I (claims 1 to 8 and 12 to 16) filed 6/29/05 to the species elected of species of figures 1 to 7 filed 4/4/05 has been acknowledged.

Claims 9-11 have been cancelled.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern and **array of solder balls disposed on an outside surface of the integrated circuit package** in claims 1 and 12 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the rem ning figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 1 to 8 and 12 to 16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 12, it is unclear and confusing to where the "an integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern and array of solder balls disposed on an outside surface of the integrated circuit package" with the other claimed elements.

Any of claims 1 to 8 and 12 to 16 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 to 6, 7, 12, 14 and 15, insofar as they can be understood, are rejected under 35 U.S.C. 102(e) as bei anticipated by Chakravorty (U.S. Patent # 6,970,362 B1).

1. Chakrovorty (figures 1 to 8) specifically figure 2 show an assembly, comprising: an integrated circuit die **40** having an array of micro-bumps **42** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **60** having an array of landing pads **61,63,65,67** disposed on an inside surface of the integrated circuit package in a second pattern and array of solder balls **142** disposed on an outside surface of the integrated circuit package, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure **50** disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad **44** located opposite to the first position and to a second landing pad **44** in the array of landing pads.

[0034] When the IC package is assembled, the lands 44 of interposer 50 are coupled to solder bumps 42 on IC die 40, and the lands 56 of interposer 50 are coupled to solder bumps 58 on primary substrate 60.

2. The assembly of claim 1, Chakrovorty show wherein a line extending through the first micro-bump in a direction orthogonal to the surface of the integrated circuit does not extend through the second landing pad of the integrated circuit package.

3. The assembly of claim 2, Chakrovorty show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the interposing structure has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the interposing structure have roughly identical surface areas.

4. The assembly of claim 3, Chakrovorty show wherein the interposing structure includes no transistor and no PN junction.

5. The assembly of claim 4, Chakrovorty show wherein the interposing structure comprises an array of micro-bumps, wherein the array of micro-bumps of the interposing structure has a pattern that is substantially identical to the second pattern of the landing pads on the inside surface of the integrated circuit package.

6. The assembly of claim 5, Chakrovorty show wherein the interposing structure includes a layer comprising epoxy and fiberglass.

8. The assembly of claim 5, Chakrovorty show wherein the first micro-bump is coupled to the first landing pad at least in part by a conductor disposed in the interposing structure, wherein the conductor disposed in the interposing structure extends in a direction parallel to the surface of the integrated circuit.

12. Chakrovorty (figures 1 to 8) specifically figure 2 show an assembly, comprising: an integrated circuit die **40** having an array of micro-bumps **42** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **60** having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially

identical patterns; the means **46** for coupling a first micro-bump in a first position in the array of microbumps to a first landing pad disposed opposed the first position and to a second landing pad located in a different position in the array of landing pads, the means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package.

14. The assembly of claim 12, Chakrovorty show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the means has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the means have roughly identical surface areas.

15. The assembly of clair 12, Chakrovorty show wherein the means has a planar form and is less than 500 microns thick.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 16, insofar as it can be understood, is rejected under 35 U.S.C. § 103(a) as being unpatentable over Chakravorty (U.S. Patent # 6,970,362 B1) in view of Berlin et al. (U.S. Patent # 6,104,082).

Chakravorty show the features of the claimed invention as detailed above, but fail to explicitly show wherein the integrated circuit die is an application specific integrated circuit (ASIC).

Berlin et al. show a metallization structure for altering connections. Specifically, Berlin et al. (figures 1 to 13b) specifically figure 2b discloses an assembly, comprising: an integrated circuit die (chips 1-6) having an array of micro-bumps **62** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **68** having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure **60'** disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed in a different position in the array of landing pads, wherein the integrated circuit die **(chips 1-6)** is an application specific integrated circuit (ASIC) for the purpose of providing an electronic module that permits changing connections while retaining a constant interface to the electronic module.

(32) The tailorable metallization of the present invention also provides a scheme for rapidly creating or altering circuit configurations; in essence application specific integrated circuits are quickly fabricated by selecting and deselecting circuits with the metallization tailoring methods disclosed herein. While it would be advantageous to test circuit elements first to ensure the functionality of the included circuits before finalizing the metallization, these ASIC circuits could also be built with the tailorable wiring of the present invention without the intermediate test. The wiring can be tailored by methods such as opening fuses, providing ribbon connections, providing bump connections, or providing photolithographically formed shapes as described herein above. In this case, defective circuits would be included and would result in yield loss but other functional chips would be fabricated in much less time than would be required to provide masks.

Therefore, it would have been obvious to one of ordinary skill in the art to use Berlin et al.'s ASIC chip type t. nodify Charkravorty's chip for the purpose of providing an electronic module that permits changing connections while retaining a constant interface to the electronic module.

Claims 7 and 13, insofar as they can be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (U.S. Patent # 6,970,362 B1) in view of Vafi et al. (U.S. Patent # 5,474,458).

Chakravorty show the features of the claimed invention as detailed above, but fail to explicitly show wherein the interposing structure includes a bypass capacitor.

Vafi et al. is cited for showing interconnect carriers having high density vertical connectors. Specifically, Vafi et al. (figures 1 to 10C) specifically figures 2 and 3 show an assembly, comprising: an integrated circuit die 1 having an array of micro-bumps 15 disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package 3 having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; an interposing structure 10 disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad located opposite to the first position and to a second landing pad in the array of landing pads and the interposing structure includes a bypass capacitor for the purpose of increasing the density of electrical interconnects of interposers and like devices.

Therefore, it would have been obvious to one of ordinary skill in the art to use Vafi et al.'s bypass capacitor included in the interposer to modify Charavorty's interposer for the purpose of increasing the density of electrical interconnects of interposers and like devices.

(6) For electrical coupling, a plurality of solder bumps are typically disposed on the pads of either the IC chip or the interposer'stop surface (or on both sets of pads). Likewise, a second plurality of solder bumps are typically disposed on the pads of either the major substrate or the interposer's bottom surface (or on both sets of pads). The interposer is then brought into alignment and initial contact with the IC chip and major substrate such that corresponding pads are aligned and separated by a corresponding solder bump. The solder bumps are then reflowed by heat to wet and make an adhesive and electrical contact with their corresponding pads. The reflow allows each solder bump to independently change its dimensions so at to compensate for any height variations which may be caused by warpage in the interposer's substrate, the IC chip, or the major substrate, or which may be caused by size variations in the solder bumps. For each of the interposer, IC chip, and major substrate, warpage may cause a 2 .mu.m (micron) to 4 .mu.m height difference between the high and low spots within a .about. 1.0 square centimeter area thereof. Accordingly, for a one centimeter square chip, there may be up to a 4 .mu.m to 8 .mu.m variation in the spacing between the interposer and the IC chip when they are brought into contact. The solder bumps are generally made large enough to compensate for such height variations.

(7) The above-described type of interposer has a number of limitations which discourage its use for high-performance IC chips. First, such IC chips often consume large amounts of power, which raises the temperatures of the chips, causing their dimensions to expand. The thermally induced expansion generates mechanical stresses between the IC chip and the interposer and, as the interposer heats up, stresses between the interposer and the major substrate. These stresses may be sufficient to cause weak solder bumps to break away from their corresponding pads, resulting in a loss of electrical connection. Additionally, as the system undergoes thermal cycling, repeated stress can cause metal fatigue leading to failure of one or more of the bump/pad joints which couple the chip, interposer, and

supporting substrate to one another. One prior art way of mitigating the mechanical stresses is to construct the interposer from a material which has a coefficient of thermal expansion (CTE) near that of the IC chip. However, mechanical stresses may still occur between the interposer and the chip each time the IC chip is "powered-up" if a large transient temperature difference develops between the IC chip and the interposer during start up. Additionally, a similar thermal transient may occur between the interposer and the major substrate.

(8) In addition, because of its relatively large surface area, a typical high performance IC chip often has a large warpage across its active surface. If large enough, this warpage can prevent one or more solder bumps from contacting corresponding pads. The chance of contact failure increases as the combined warpage of the IC chip and interposer increases. Additionally, the combined warpages cause variations in the heights and widths of the solder bumps, which in turn causes the thermally-induced mechanical stresses to concentrate at a relatively small number of solder bumps, particularly those with low aspect ratios. This concentration increases the chance of a solder bump failing. Similar warpage effects occur for the interface between the interposer and major substrate. To minimize the warpage effects for both interfaces of the interposer, and thereby minimize the chances of a solder bump failure occurring at either of the interfaces, the interposer should have the smallest possible warpage. Unfortunately, with current manufacturing processes, the yield of interposers with low-warpage decreases as the size of interposers increases, thereby increasing the cost of manufacturing them.

(12) In addition to the above interconnect issues, many high performance IC chips require at least one power supply which can supply large transient currents, as for example caused by simultaneous switching of digital circuity, without a significant change in the voltage it provides to the IC chip. One way of accommodating large transient currents is to couple a low inductance, high-value bypass capacitor between the power supply and a reference potential (e.g., ground), placing the bypass capacitor as close to the IC chip as possible. Many rigid, ceramic-substrate interposers incorporate bypass capacitors within their substrates. However, such a capacitor generally occupies a relatively large area, which would prevent the incorporation of many such capacitors on the same interposer

unless more layers were added to the interposer, at a further cost, to distribute the capacitors over several layers. To the inventors' knowledge, many, if not all, flexible film interposers do not incorporate bypass capacitors. It is believed that the incorporation of bypass capacitors on such interposers would present major fabrication issues which the art has not heretofore addressed.

(16) There is a further need to have a high-value bypass capacitance integrated on the interposer, or interconnect structure, along with the large number of interconnects.

(9) Interconnect carrier 10 may further comprise one or more capacitor structures 80, which may be used as bypass capacitance between adjacent power and ground lines. Capacitor structure 80 comprises a first conductive layer, or electrode, formed over a portion of one surface of supporting layer 20, a dielectric layer formed over a portion of the first conductive layer, and a second conductive layer formed over a portion of the dielectric layer. Each of the conductive layers is coupled to at least one via 30. The conductive layers and dielectric layer of the capacitor structure layer 80 are relatively thin in comparison to the thickness of supporting layer 20. These layers are shown in detail in the embodiments of the present invention shown in FIG. 4B. Capacitor 80 may, for example, be formed with a capacitance of approximately 20-200 nanofarads per square centimeter within a substantially rectangular area measuring between approximately 200 .mu.m to 350 .mu.m on a side.

Response

Applicant's arguments filed 10/10/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/653,758,774,778,737,738,734,686,685,723,691,774,692,693,700,e25.013,e23.125,e23.079,e23.026,e23.e23.063.e23.101,e23.181,e23.069,e23.126 361/306.3,312,313,321.1,321.4,763	9/11/05 4/13/06 7/24/06 12/23/06
Other Documentation: foreign patents and literature in 257/653,758,774,778,737,738,734,686,685,723,691,774,692,693,700,e25.013,e23.125,e23.079,e23.026,e23.e23.063.e23.101,e23.181,e23.069,e23.126 361/306.3,312,313,321.1,321.4,763	9/11/05 4/13/06 7/24/06 12/23/06
Electronic data base(s): U.S. Patents EAST	9/11/05 4/13/06 7/24/06 12/23/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
12/23/06